REMARKS

Claims 1-3, 6, 9-11, 14, and 17 are amended. Claims 1-20 remain in the Application. Reconsideration of the pending claims is respectfully requested in view of the above amendments and the following remarks.

I. In the Specification

Applicants have amended the typographical errors on page 2, lines 4-15 of the specification. Approval of this amendment is respectfully requested.

II. Claim Objections

Claims 6 and 14 are objected to because of informalities. Applicants replace the term "form1" with "form' as requested by the Examiner. Approval of this amendment is respectfully requested.

III. Claims Rejected Under 35 U.S.C. § 112

Claims 3, 11 and 19 stand rejected under 35 U.S.C. § 112, second paragraph as being incomplete for omitting essential structural cooperative relationships of elements. Specifically, the Examiner indicates that the "earlier one external clock period" relationship is unclear. Applicants amend Claims 3, 11, and 19 to recite "earlier than the tRCD timing by one external clock period." The amendments are supported by the specification and the drawings, e.g., Figures 9 and 10. Accordingly, reconsideration and withdrawal of the § 112 rejection of Claims 3, 11, and 19 are requested

IV. Claims Rejected Under 35 U.S.C. § 102

Claims 1-5 and 17-20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2003/0090307A1 to Shin ("Shin").

To anticipate a claim, the Examiner must show that a single reference teaches each of the elements of that claim. Among other elements, amended Claim 1 recites:

> "a control block, in response to the plurality of
> delayed clock signal, for outputting one of the plurality of

internal instructions at a first predetermined timing which is earlier than the timing of starting the operation according to an additive latency" (emphasis added).

Shin does not disclose the control block for outputting one of the plurality of internal instructions at a first predetermined timing which is earlier than the timing of starting the operation according to an additive latency.

Applicants' specification defines the additive latency, in plain English, as the number of clock cycles between the input of an external instruction (e.g., read/write) and a tRCD timing (page 2, line 24 - page 3, line 2). The tRCD timing, as used consistently in the specification, means the time when the column address strobe (CAS) is generated after the generation of the row address strobe (RAS) (page 18, lines 14-18). Thus, the additive latency, as described in the specification and shown in Figures 6, 9, and 10, is the time period between the input of an external instruction (e.g., read/write) and the generation of a CAS.

According to the present invention disclosed in the specification, the control block outputs the internal instructions at a tRCD timing when there is no additive latency (i.e., the additive latency is 0). Otherwise, when the additive latency is not 0, the internal instructions are outputted at a predetermined timing earlier than the tRCD timing. Thus, as recited in Claim 1, the internal instruction is outputted at a time earlier than the timing of starting the operation according to an additive latency.

However, according to the memory device of Shin, the delay time of an output control clock signal varies in response to a CAS latency, which is the number of clock cycles from the time an external instruction is inputted to the memory device to the time a data sequence is outputted to an external circuit in response to the external instruction. Shin does not disclose the timing of an internal instruction in relation to an additive latency. As explained above, the CAS latency is different from the claimed additive latency. Thus, Shin does not teach each of the elements of amended Claim 1.

Analogous discussions apply to independent Claim 17, which is amended to include similar limitations. In regard to Claims 2-5 and 18-20, these claims depend from Claims 1 and 17, respectively, and incorporate the limitations thereof. Thus, for at least

the reasons mentioned above in regard to Claims 1 and 17, Shin does not anticipate these claims. Accordingly, reconsideration and withdrawal of the § 102 rejection of Claims 1-5 and 17-20 are respectfully requested.

V. Claims Rejected Under 35 U.S.C. § 103(a)

Claims 6-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2003/0090307A1 to Shin ("Shin") in view of Applicant's Admitted Prior Art ("AAPA").

To establish a *prima facie* case of obviousness, the relied upon references must teach or suggest every limitation of the claim such that the invention as a whole would have been obvious at the time the invention was made to one skilled in the art.

Independent Claim 9 is amended to include the limitations of "a control block, ... for outputting one among the plurality of internal instructions at a first predetermined timing which is earlier than the timing of starting the operation according to an additive latency." Thus, for similar reasons discussed above in regard to Claim 1, Shin does not teach or suggest each of the elements of Claim 9. Claims 6-8 and 10-16 depend from Claims 1 and 9, respectively, and incorporate the limitations thereof. Thus, for at least the reasons mentioned above in regard to Claims 1 and 9, Shin does not teach or suggest each of the elements of these claims.

AAPA does not cure the deficiency of Shin. As shown in Figures 5 and 6 of AAPA, the internal instruction (Com_int) is generated after the tRCD timing, that is, after the timing of starting the operation regardless of the amount of additive latency. Thus, the cited references do not, separately or in combination, teach or suggest each of the elements of Claims 1 and 9, as well as their dependent claims, namely, Claims 6-8 and 10-16.

One of the advantages of the claimed invention is to generate corresponding internal instructions faster as the external instructions are input faster. Accordingly, the semiconductor memory device of the claimed invention increases a timing margin, which is used for preventing a timing error and improving an address access timing

tAA. The semiconductor memory device of the claimed invention operates more stably. As a result, a fractional yield of the semiconductor memory device is increased.

Therefore, the cited references do not teach or suggest each of the elements of Claims 6-16. Accordingly, reconsideration and withdrawal of the § 103 rejection of Claims 6-16 are respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims are now in condition for allowance and such action is earnestly solicited at the earliest possible date. If there are any additional fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666.

Respectfully submitted,

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Dated: January 5, 2007

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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Amber D. Saunders 1/9/2007

Amber D. Saunders Date